CLAIM AMENDMENTS

110. A ~~medium~~ memory that is readable by an apparatus having a processor and having stored thereon a processor-executable instruction, which if executed by the processor, causes the processor to perform a method comprising:

storing bits [31-0] of a source value into bit storage locations [63-32] and [31-0] of a destination register;

storing bits [95-64] of the source value into bit storage locations [127-96] and [95-64] of the destination register, wherein the instruction implicitly indicates the bits of the source value which are to be stored in the destination register.

111. The ~~medium~~ memory of claim 110 wherein the source value is stored in a memory location.

112. The ~~medium~~ memory of claim 110, wherein the source value is stored in a register.

113. A medium selected from a memory and a cache that is readable by an apparatus having a processor and having stored thereon a processor-executable instruction, which if executed by the processor causes the processor to perform a method comprising:

storing bits [63-32] of a source value into bit storage locations [31-0] and [63-32] of a destination register;

storing bits [127-96] of the source value into bit storage locations [127-96] and [95-64] of the destination register, wherein the instruction implicitly indicates the bits of the source value which are to be stored in the destination register.

114. The medium of claim 113 wherein the source value is stored in a memory location.

115. The medium of claim 113, wherein the source value is stored in a register.

116. A non-transitory medium that is readable by an apparatus having a processor and having stored thereon a processor-executable instruction, which if executed by the processor causes the processor to perform a method comprising:

storing only bits [63-32] of a source value into bit storage locations [127-96] and [63-32] of a destination register;

storing only bits [31-0] of the source value into bit storage locations [31-0] and [95-64] of the destination register, wherein the instruction implicitly indicates the bits of the source value which are to be stored in the destination register.

117. The medium of claim 116 wherein the source value is stored in a memory location.

118. The medium of claim 116, wherein the source value is stored in a register.

119. A medium selected from a memory and a cache that is readable by an apparatus having a processor and having stored thereon a processor-executable instruction, which if executed by the processor, causes the processor to perform a method comprising:

storing bits [31-0] of a source value into bit storage locations [31-0] of a destination register;

duplicating bits from the bit storage locations [31-0] to bit storage locations [63-32] of the destination register;

storing bits [95-64] of the source value into bit storage locations [95-64] of the destination register; and

duplicating bits from the bit storage locations [95-64] to bit storage locations [127-96] of the destination register, wherein the instruction implicitly indicates the bits of the source value which are to be stored in the destination register.

120. A tangible medium that is not a propagated signal that is readable by an apparatus having a processor and having stored thereon a processor-executable instruction, which if executed by the processor causes the processor to perform a method comprising:

storing bits [63-32] of a source value into bit storage locations [63-32] of a destination register;

duplicating bits from the bit storage locations [63-32] to bit storage locations [31-0] of the destination register;

storing bits [127-96] of the source value into bit storage locations [127-96] of the destination register; and

duplicating bits from the bit storage locations [127-96] to bit storage locations [95-64] of the destination register, wherein the instruction implicitly indicates the bits of the source value which are to be stored in the destination register.

125. The ~~medium~~ memory of claim 110, in which the first instruction indicates operands consisting of a single source operand corresponding to the source value and a single destination operand corresponding to the destination register.

126. The medium of claim 113, in which the first instruction indicates operands consisting of a single source operand corresponding to the source value and a single destination operand corresponding to the destination register.

127. The medium of claim 116, in which the first instruction indicates operands consisting of a single source operand corresponding to the source value and a single destination operand corresponding to the destination register.

129. The ~~medium~~ memory of claim 110, in which the bits of the source value to be stored in the destination register are fixed for the instruction.

130. The medium of claim 113, in which the bits of the source value to be stored in the destination register are fixed for the instruction.

131. The medium of claim 116, in which the bits of the source value to be stored in the destination register are fixed for the instruction.

(Cancelled) ~~132. The medium of claim 110, wherein the medium comprises a memory.~~

133. The medium of claim 113, wherein the medium comprises a memory.

134. The medium of claim 116, wherein the medium comprises a memory.